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10/004,039	11/14/2001	Craig Nemecek	CYPR-CD01222M	1791

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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,039	NEMECEK ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-13 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,11-13 and 15-18* is/are rejected.

7)☒ Claim(s) *3 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 were rejected in office action of 22 November 2005.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 January 2006 has been entered.

Applicants' response has cancelled claims 2, 7, 14, and 19; and amended claims 1, 3, 8, 11, 12, 15, and 17. Claims 1, 3-6, 8-13, and 15-18 are currently pending in this application.

Claims 1, 3-6, 8-13, and 15-18 have been rejected.

Claim Rejections - 35 USC § 112

The previous rejections under 35 U.S.C. § 112 have been withdrawn in response to Applicants' response.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

1. Claims 1, 4-6, 11-13, and 15-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,911,059 to Profit, Jr. (Profit).

Regarding claim 1, Profit teaches an in-circuit emulation system including:

A microprocessor (column 6, lines 5-24, especially lines 18-19), the microprocessor has a clock count and therefore a clock (column 12, lines 24-35);

A virtual microprocessor (referred to as a processor model shell 212) (column 6, lines 25-32) running in lock-step with the microprocessor (column 11, lines 40-43);

A host computer running in-circuit emulation debug software (column 6, lines 25-60), the host computer being in communication with the virtual microcontroller (Fig. 7, reference 220; column 5, line 58 – column 6, line 4); and

A gatekeeper circuit (referred to as RUN/HALT controller 240) coupled to the virtual microcontroller and the microcontroller (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as time keeper circuit 232) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Profit's preferred embodiment comprises a single clock running the gatekeeper circuit and microcontroller [*"A clock 242 drives the latch control circuit 248, this clock typically being the same clock which drives the processor 204"* (column 9, lines 29-31)] but in doing so, clearly suggests the use of separate clocks as an alternative embodiment. Thus Profit may not disclose this claimed limitation, however Profit clearly teaches and suggests this limitation.

Official Notice is taken that the term microcontroller refers to a single unit usually comprising central processing unit, memory, and I/O ports. Applicants have not seasonably challenged this use of Official Notice.

As Profit teaches an emulator unit that contains at least these features (Fig. 7, reference 202), it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention that Profit's emulator is readily adaptable to accept microcontrollers, as would be desired by a person whose goal it is to develop and debug code for microcontrollers.

Regarding claim 4, Profit teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Regarding claims 5 and 6, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding claim 11, Profit teaches an in-circuit emulation system with a gatekeeper circuit (referred to as RUN/HALT controller 240) (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as time keeper circuit 232) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Profit also teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Profit's preferred embodiment comprises a single clock running the gatekeeper circuit and microcontroller [*"A clock 242 drives the latch control circuit 248, this clock typically being the same clock which drives the processor 204"* (column 9, lines 29-31)] but in doing so, clearly suggests the use of separate clocks as an alternative embodiment.

Profit also teaches sending a signal to the virtual microcontroller to resume its operation, functionally equivalent to providing a clock signal (column 10, lines 4-23).

Profit does not explicitly recite "permitting the host computer to query memory locations and registers of the virtual microcontroller", however Profit does explicitly recite that the host computer contains software debugging tools (column 6, lines 49-60). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine Profit's explicit suggestion, in combination with his own knowledge of the particular art, to include the memory and register probing means that are both well known in the art and necessary to adequately debug software for the microcontroller.

Regarding claims 12 and 13, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding claim 15, Profit teaches an in-circuit emulation system with a gatekeeper circuit (referred to as RUN/HALT controller 240) (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as time keeper circuit 232) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Profit also teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the

processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed limitation of "determining that a watchdog timer event has occurred in a microcontroller".

Profit also teaches a virtual microprocessor (referred to as a processor model shell 212) (column 6, lines 25-32) running in lock-step with the microprocessor (column 11, lines 40-43);

Profit also teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Profit's preferred embodiment comprises a single clock running the gatekeeper circuit and microcontroller [*"A clock 242 drives the latch control circuit 248, this clock typically being the same clock which drives the processor 204"* (column 9, lines 29-31)] but in doing so, clearly suggests the use of separate clocks as an alternative embodiment.

Profit also teaches notifying a host computer running in-circuit emulation software that a watchdog timer event has occurred (column 11, lines 56-61).

Regarding claim 16, Profit does not explicitly recite "permitting the host computer to query memory locations and registers of the virtual microcontroller", however Profit does explicitly recite that the host computer contains software debugging tools (column 6, lines 49-60). It would have been obvious to a person of ordinary skill in the art at the time of Applicants'

invention to combine Profit's explicit suggestion, in combination with his own knowledge of the particular art, to include the memory and register probing means that are both well known in the art and necessary to adequately debug software for the microcontroller.

Regarding claims 17 and 18, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Response to Arguments

In response to the previous rejections, Applicants argue primarily that:

> Applicants respectfully assert that Profit fails to suggest, teach, or describe the limitation "a virtual microcontroller running in lock-step synchronization with the microcontroller" as recited in independent Claim 1.

The Examiner respectfully traverses this argument as follows.

Profit discloses:

> Setting the time interval to zero would cause synchronization to occur at the execution of each instruction. Thus, with this method the synchronization is not periodic. (column 11, lines 40-43)

This and related portions of Profit clearly teach lock-step synchronization. Applicants' arguments are not directed toward "a virtual microcontroller" or "the microcontroller." Applicants' arguments rely on the disclosure of the application rather than the claimed limitations. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See MPEP 2145 (VI).

Applicants further argue that:

> Moreover, by teaching that the target program and target circuitry do not operate in lock-step synchronization as claimed, Profit effectively teaches away from the claimed embodiments.

The Examiner respectfully traverses this argument as follows.

As shown above, Profit does teach the claimed lock-step synchronization feature. However, the Examiner is unaware of support in the MPEP for Applicants' argument on the basis of "teaching away," even assuming arguendo that the alleged deficiencies of Profit are true. Please see MPEP 2123 (II). Applicants have provided no evidence that Profit teaches a lock-step synchronization as somehow inferior, and indeed Profit teaches lock-step synchronization.

Applicants further argue that:

> Applicants respectfully assert that Profit fails to suggest, teach, or describe the limitation "a gatekeeper clock running independent of the microcontroller clock" as recited in independent Claim 1.

The Examiner respectfully traverses this argument as follows.

As cited, above, Profit discloses:

> A clock 242 drives the latch control circuit 248, this clock typically being the same clock which drives the processor 204. (column 9, lines 29-31)

Profit discloses a preferred embodiment, however the MPEP provides clear instruction that non-preferred and alternative embodiments constitute prior art. See MPEP 2123 (II). Profit's disclosure is not limited to merely using the same clock in all situations. Profit discloses that typically the same clock is used. In doing so, Profit clearly teaches that, in the atypical situation, separate clocks are used. Therefore, Profit teaches a gatekeeper clock running independent of the microcontroller clock. There are myriad reasons for using separate clocks on separate devices known in the art, such as simplicity of design, economy, performance, or flexibility. US Patent No. 5,371,878 to Coker, which is not being relied upon to form this rejection, discloses a related invention that comprises separate clocks on separate devices (ex. FIG 1., references 10 and 36).

Applicants further present analogous arguments to those shown above that the alleged deficiencies of Profit "teach away" from the claimed invention. The Examiner finds the Profit overcomes these alleged deficiencies and does not find support in the MPEP for Applicants' use of the phrase "teaches away" under the present circumstances. Applicants have provided no evidence that Profit teaches separate clocks as somehow inferior, and indeed Profit teaches the use of separate clocks.

Applicants present analogous arguments for independent claims 11 and 15, and for the pending dependent claims by virtue of being dependent upon an allowable base claim. These arguments have been fully considered as above.

Applicants' arguments have been fully considered but have been found unpersuasive.

Allowable Subject Matter

2. Claims 3 and 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or suggest "means for replacing the microcontroller clock signal with the gatekeeper clock signal for clocking the virtual microcontroller when a watchdog event occurs" in combination with the other recited limitations of claim 3. Claims 8-10 are dependent from an allowable base claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 4/7/06
Primary Examiner
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